

1/15

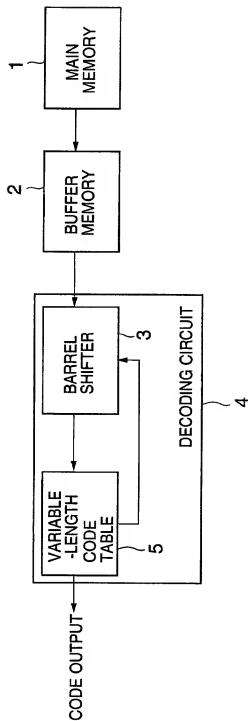


FIG. 1
PRIOR ART

104021 18000001

2/15

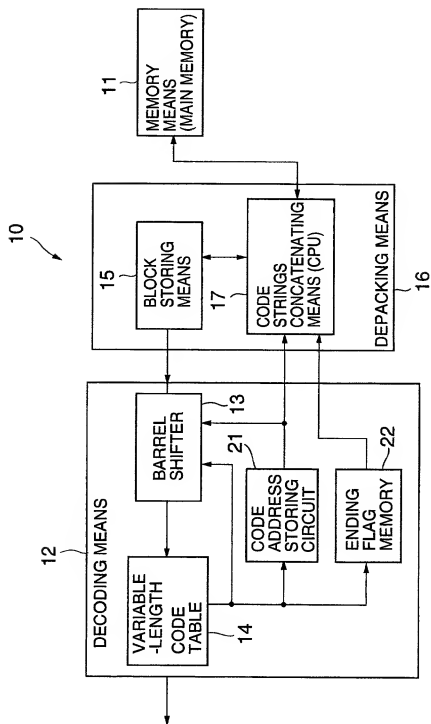


FIG.2

3/15

ITEMS	BUFFER MEMORY CAPACITY	ACCESS FREQUENCY OF MAIN MEMORY
GENERAL METHOD	(4400bit)	—
JPA.No 8-275162 (WITH BUFFER)	(3040bit)	LOW
JPA.No 8-275162 (WITHOUT BUFFER)	(~0bit)	HIGH
EMBODIMENT OF THIS INVENTION	(112bit)	LOW

FIG.3

104021* 13000001

4/15

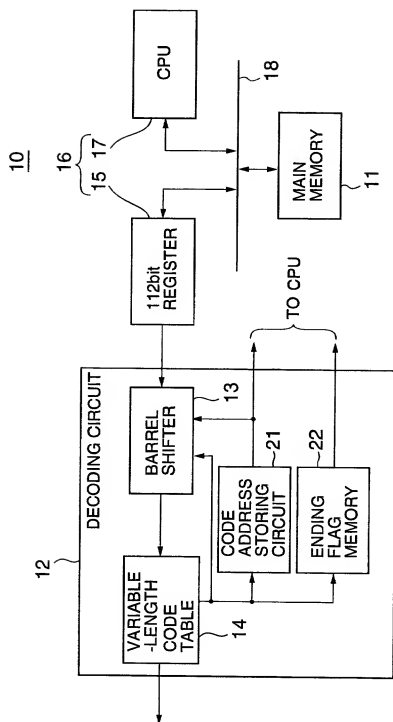


FIG.4

FIG. 4

5/15

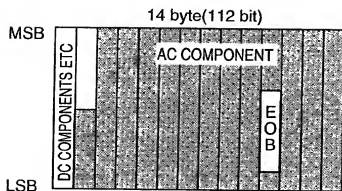


FIG.5

LONGEST REMAINDER WHEN EOB IS DETECTED

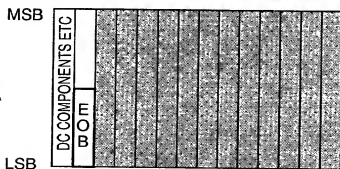


FIG.6A

THERE IS EOB IMMEDIATELY AFTER DC COMPONENTS.
 16 BIT ARE EMPTY, OTHER IS REMAINDER

LONGEST REMAINDER WHEN EOB IS NOT DETECTED

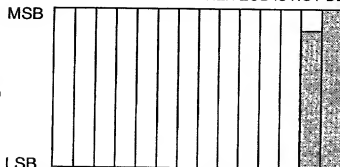
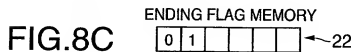
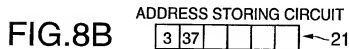
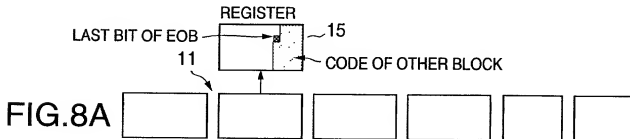
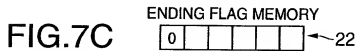
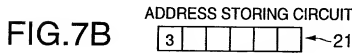
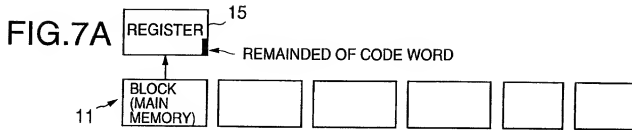


FIG.6B

WHEN LONGEST CODE (16 BIT) IS NOT INCLUDED,
 REMAINDER IS 15 BIT.

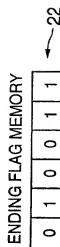
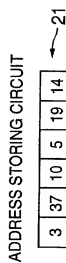
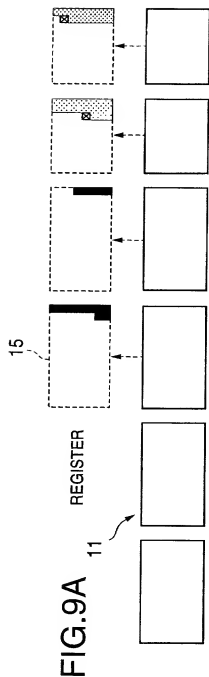
10000001 12000001

6/15



10000001 1800001

7/15



10402478000001

8/15

104021" 18000001

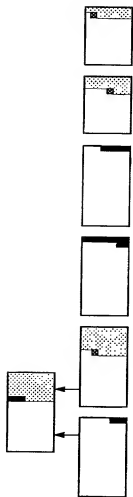


FIG. 10A

ADDRESS STORING CIRCUIT

3 37 10 5 19 14 ~ 21

ENDING FLAG MEMORY

0 1 0 0 1 1 ~ 22

FIG. 10B

FIG. 10C

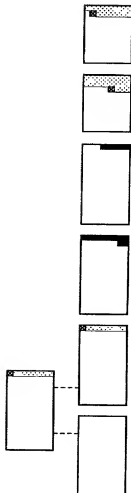


FIG. 11A

ADDRESS STORING CIRCUIT

0 7 10 5 19 14 ~ 21

ENDING FLAG MEMORY

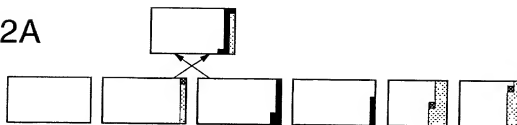
1 1 0 0 1 1 ~ 22

FIG. 11B

FIG. 11C

9/15

FIG.12A



ADDRESS STORING CIRCUIT

FIG.12B

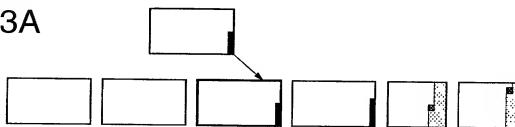
0 7 10 5 19 14 ~ 21

ENDING FLAG MEMORY

FIG.12C

1 1 0 0 1 1 ~ 22

FIG.13A



ADDRESS STORING CIRCUIT

FIG.13B

0 0 4 5 19 14 ~ 21

ENDING FLAG MEMORY

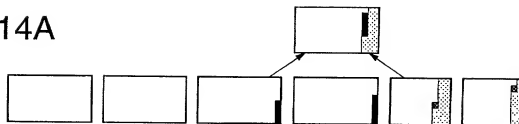
FIG.13C

1 1 0 0 1 1 ~ 22

104021-18000001

10/15

FIG.14A



ADDRESS STORING CIRCUIT

FIG.14B

0	0	4	5	19	14
---	---	---	---	----	----

 ~ 21

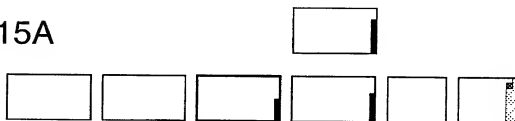
ENDING FLAG MEMORY

FIG.14C

1	1	0	0	1	1
---	---	---	---	---	---

 ~ 22

FIG.15A



ADDRESS STORING CIRCUIT

FIG.15B

0	0	6	5	0	14
---	---	---	---	---	----

 ~ 21

ENDING FLAG MEMORY

FIG.15C

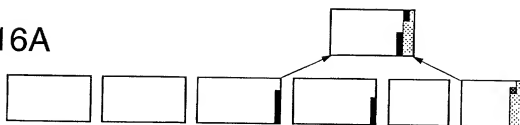
1	1	0	0	1	1
---	---	---	---	---	---

 ~ 22

10000081-120401

11/15

FIG.16A



ADDRESS STORING CIRCUIT

FIG.16B

0	0	6	5	0	14
---	---	---	---	---	----

 ~ 21

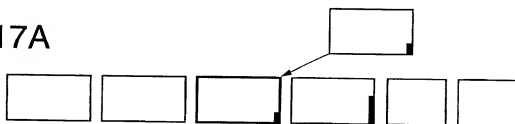
ENDING FLAG MEMORY

FIG.16C

1	1	0	0	1	1
---	---	---	---	---	---

 ~ 22

FIG.17A



ADDRESS STORING CIRCUIT

FIG.17B

0	0	2	5	0	0
---	---	---	---	---	---

 ~ 21

ENDING FLAG MEMORY

FIG.17C

1	1	0	0	1	1
---	---	---	---	---	---

 ~ 22

104021-1800001

12/15

MEMORY ACCESS FREQUENCY IN PRIOR ART

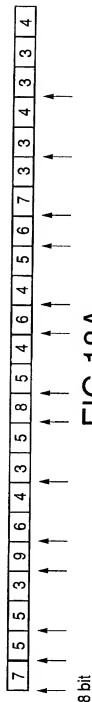
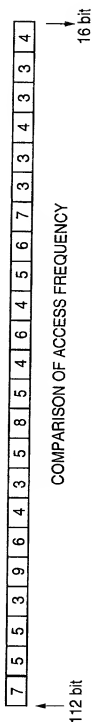


FIG.18A

MEMORY ACCESS FREQUENCY OF THIS INVENTION



COMPARISON OF ACCESS FREQUENCY

FIG.18B

13/15

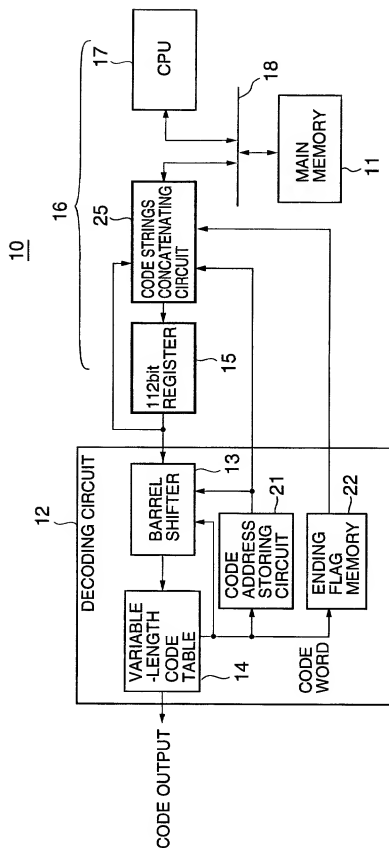


FIG.19

14/15

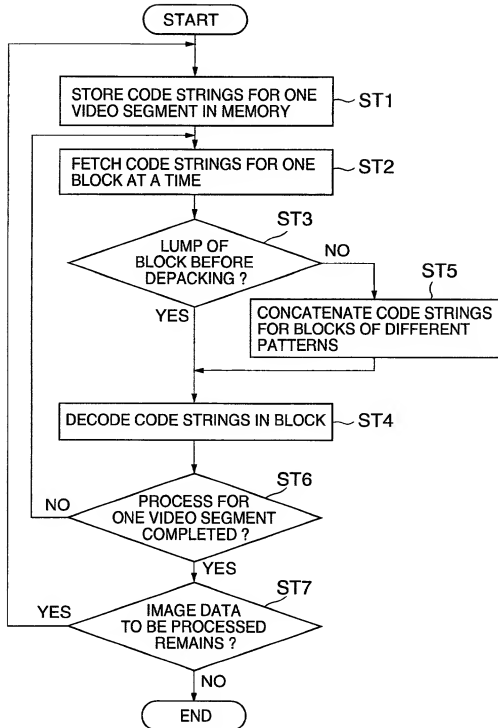


FIG.20

15/15

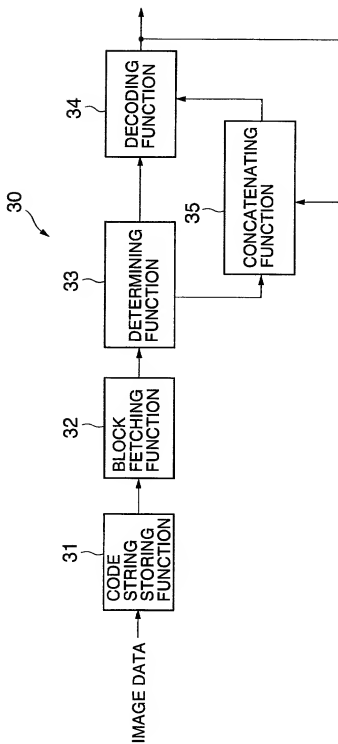


FIG.21

104021*18000001